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PATENT

IN THE SPECIFICATION

On page 1, please replace the paragraph immediately following the title **CROSS-REFERENCE TO RELATED APPLICATION,** as follows:

This Application relates to U.S. Patent No. 7,002,499, issued February 21, 2006, entitled Clocked D/A Converter, formally co-pending U.S. Patent Application Serial No. 10/763,071, by Todd Kaplan and Albert E. Cosand, filed on the same date of the present Application, the disclosure of which is incorporated herein by reference in its entirety.

Please amend the paragraph on page 2, beginning at line 4 as follows:

Delta-sigma modulators allow for the use of low-resolution components running at a higher sampling rate to provide a high resolution ADC converter at a lower sampling rate. Delta-sigma modulators allow for lower costs and higher accuracy than could otherwise be achieved without a delta-sigma modulator. ~~(True, but of limited relevance to the subject of the patent application)~~ Sigma-delta modulator (ADC) converters include a delta-sigma modulator and a digital filter, which processes the output thereof.

Please amend the paragraph on page 2, beginning at line 12 as follows:

A highly precise current switch is needed for current switching of continuous-time analog to digital converters (ADCs) employed in delta-sigma modulators. A simple differential pair of transistors driven by a clocked latch has been used in the past to provide current switching for ADCs used in delta-sigma modulators. However, simple differential pair current switches may be sensitive to thermal history and produce an effect known as 'intersymbol interference'). That is, if the latch has been switched to one state for a sufficient period of time, one transistor heats more than the other and changes its switch threshold. When the signal driving the switch has a non-zero risetime, this ~~This~~ has the

effect of changing the timing of the switch transition. Such thermal errors are difficult to characterize and compensate for.

Please amend the paragraph on page 2, beginning at line 28 as follows:

More recently, Adams *et al.* described a scheme with two interleaved RZ DACs to provide a more continuous output than does a single RZ DAC. (See "A 113dB SNR Oversampling DAC with Segmented Noise-Shaped Scrambling", IEEE Solid-State Circuits Conference, 1998.) This approach consumes additional current, is subject to clock jitter, and does not cancel all thermal effects.

Please amend the paragraph on page 3, beginning at line 4 as follows:

A co-pending Application entitled "Clocked D/A/ Converter," also filed January 21, 2004 as U.S. Patent Application Serial No. 10/763,071, now U.S. Patent No. 7,002,499, issued February 21, 2006 ~~(Attorney Docket No. B-4850-620354)~~ by Todd Kaplan and Albert E. Cosand, the teachings of which are hereby incorporated herein by reference, describes a latch used as a DAC switch. Unfortunately, in its simplest form, this circuit is sensitive to the voltage swing at the output summing nodes. This sensitivity can be alleviated by the addition of a common-base output stage, but that may increase the required supply voltage.

Please divide the paragraph beginning on page 6, line 24 into 2 paragraphs and amend as follows:

Thus, a continuous feedback path is provided to the loop filter 12 and the data fed back determines whether the feedback signal is positive or negative. As is known in the

art, a 'continuous time' DAC (digital-to-analog converter) ~~in~~ is one in which data is being output continuously up to the time of switching. **(Paragraph Division Begins Here)**

Fig. 2 is a timing diagram illustrating the operation of the switch of the present invention. The inputs are three differential signal pairs: the clock CLK/CLKX, and two copies of the data, DM/DMX and DS/DSX. As seen in Fig. 2, the two versions of the data differ in delay by one half of a clock period; DM and DS may be obtained respectively from the master and slave latches of a D flip-flop. DM changes state following a falling edge of CLK and DS changes state following a rising edge of CLK. As mentioned above, the differential pair Q1/Q2 is driven by the master latch output DM. The logic signal at the bases of Q1 and Q2 has had a half clock period to settle when CLK goes high and causes the DAC tail current to be steered through Q5 into the emitters of Q1/Q2. The current is then steered to the selected output according to the state of DM. During the time that CLK is high, DS has time to settle to its correct value so that when CLK goes low (CLKX goes high), the DAC current will be steered through Q6 to the emitters of Q3/Q4 and then to the correct output.